AMENDMENTS TO THE SPECIFICATION

Please amend the second full paragraph on page 5 as follows:

When the monitor potential VM is higher than the input potential VI, the current flowing into P-type transistor 3 becomes larger than the current flowing into N-type transistor 5, increasing the potential V3 at node N3. This reduces the current flowing into P-type transistor 8, thereby reducing the monitor potential VM. When the monitor potential VM is smaller than the input potential VI, the current flowing into P-type transistor 3 becomes smaller than the current flowing into the N-type transistor 5, reducing the potential V3 at node N3. This allows larger current to flow into P-type transistor 8, increasing the monitor potential VM. Thus, VM = VI.

Please amend the third full paragraph on page 17 as follows:

When the output potential VO is higher than the input potential VI, the gate-source voltage of N-type transistor 10 in push type drive circuit 1 becomes smaller than the threshold voltage VTN of N-type transistor ~~86~~ 10 and thus N-type transistor 10 becomes non-conductive, while the source-gate voltage of P-type transistor 58 in pull type drive circuit 65 becomes larger than the absolute value of the threshold voltage VTP of P-type transistor 58 and thus P-type transistor 58 becomes conductive, thereby reducing the output potential VO.

Please amend the last paragraph on page 19 and continuing onto page 20 as follows:

Switches S1a and S1b are connected between input node N1 and the gates of N-type transistor 5 and P-type transistor 28 of drive circuits 1 and 65, respectively. Capacitor 111a and switch S2a are connected in series between the gate of N-type transistor 5 of drive circuit 1 and

the source of N-type transistor 10 (node N10). Capacitor 111b and switch S2b are connected in series between the gate of ~~N~~ P-type transistor ~~5~~ 28 of drive circuit 65 and the source of P-type transistor 58 (node N60). Switch S3a is connected between input node N1 and a node between capacitor 111a and switch S2a. Switch S3b is connected between input node N1 and a node between capacitor 111b and switch S2b. Switches S4a and S4b are connected between respective nodes, N10 and N60, and output node N2.

Please amend the second full paragraph on page 20 as follows:

Then, when switches S1a, S2a, S1b, and S2b are turned off, the offset voltages VOFa, VOFb are retained in capacitors 111a and 111b, respectively. Then, when switches S3a, S3b are turned on, the gate voltages of N-type transistors 5 and P-type transistor 28 of drive circuits 1, 65 are given by: VI + VOFa and VI + VOFb, respectively. As a result, the output potentials V10, V60 of their respective drive circuits 1, 65 are given by: V10 = VI + VOFa – VOFa = VI and V60 = VI + VOFb – VOFb = VI, thereby eliminating the offset voltages VOFa, VOFb of their respective drive circuits 1, 65. Finally, switches S4a, S4b are turned on such that VO = VI.